

What is claimed is:

1. A pulse duty deterioration detection circuit for a to-be-monitored clock, comprising:

5 a delay circuit comprised of a general-purpose gate circuit which generates a delayed synchronous to-be-monitored clock by delaying said to-be-monitored clock by a predetermined time;

10 a latch circuit which detects based on said to-be-monitored clock and said delayed synchronous to-be-monitored clock that a value of a decrease in a pulse width to be determined by a pulse duty of said to-be-monitored clock becomes smaller than said predetermined time; and

a flip-flop circuit which samples an output signal of said latch circuit based on said to-be-monitored clock.

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2. A pulse duty deterioration detection circuit for a to-be-monitored clock, comprising:

20 a delay circuit comprised of a general-purpose gate circuit which generates a delayed synchronous to-be-monitored clock by delaying said to-be-monitored clock by a predetermined time;

25 a first latch circuit which detects based on said to-be-monitored clock and said delayed synchronous to-be-monitored clock that a value of a decrease in a pulse width to be determined by a pulse duty of said to-be-monitored clock becomes smaller than said predetermined time;

a second latch circuit which detects based on said to-

be-monitored clock and said delayed synchronous to-be-monitored clock that a value of an increase in said pulse width to be determined by said pulse duty of said to-be-monitored clock becomes greater than said predetermined time;

5       a first flip-flop circuit which samples an output signal of said first latch circuit based on said to-be-monitored clock;

10       a second flip-flop circuit which samples an output signal of said second latch circuit based on said to-be-monitored clock; and

15       a circuit which detects based on output signals of said first and second flip-flop circuits that said pulse width of said to-be-monitored clock lies within a predetermined duty range.

3. The pulse duty deterioration detection circuit according to claim 2, further comprising:

20       a first detection circuit, provided on an output side of said first flip-flop circuit, for outputting a significance signal when it is detected that said pulse duty consecutively drops plural times in a direction of reducing said pulse duty;

25       a second detection circuit, provided on an output side of said second flip-flop circuit, for outputting a significance signal when it is detected that said pulse duty consecutively drops plural times in a direction of increasing said pulse duty; and

an output circuit which outputs a signal indicating that said pulse width of said to-be-monitored clock is in a normal range when both of said first and second detection circuits output said significance signals.

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4. The pulse duty deterioration detection circuit according to claim 32, wherein said delay circuit has a delay element comprised of a plurality of general-purpose gate circuits connected in series and a switch circuit for selecting a delay time of said delay element, and said pulse duty deterioration detection circuit further comprises:

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a counter which counts up when said output circuit outputs a signal indicative of duty deterioration; and

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a decoder circuit which decodes a count value of said counter, whereby a delay time of said to-be-monitored clock is automatically changed by controlling said switch circuit for selecting said delay time of said delay element in accordance with an output signal of said decoder circuit.